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(71) Applicant *(for all designated States except US):* MOTOROLA, INC. [US/US]; 1303 East Algonquin Road, Schaumburg, IL 60196 (US).

(72) Inventors; and
(75) Inventors/Applicants *(for US only) :* DAVIS, Walter, Lee [US/US]; 10948 N.W. 3rd Street, Coral Springs, FL 33071 (US). LEONARD, Jerome, Charles [US/US]; 9305 Perth Road, Lake Worth, FL 33467 (US).

(74) Agents: DOWNEY, Joseph, T. et al.; Motorola, Inc., Patent Law Department, 8000 W. Sunrise Boulevard, Fort Lauderdale, FL 33322 (US).

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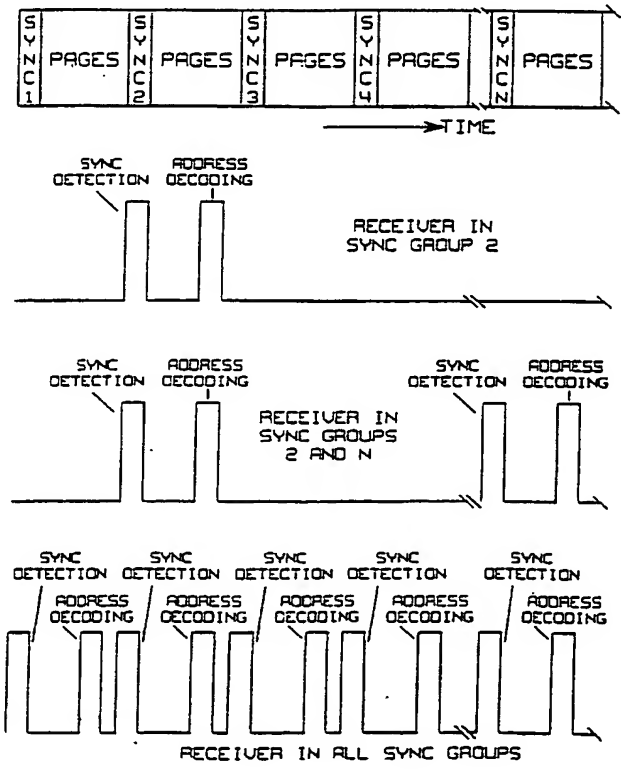
(54) Title: PAGING SYSTEM WITH ASSIGNABLE BATTERY SAVER DUTY CYCLE

(57) Abstract

A selective call communication system includes a transmitter for transmitting the selective call signals in a predetermined signalling format. A first group of selective receivers operating on the system receives and decodes the transmitted selective call signals in the predetermined signalling format. The receivers in the first group have a battery saver circuit which is operating at a first repetition rate. A second group of selective receivers also operating on the system receives and decodes the transmitted selective call signals in the predetermined signalling format. The receivers in the second group have a battery saver circuit which is operating at a second repetition rate.



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# PAGING SYSTEM WITH ASSIGNABLE BATTERY SAVER DUTY CYCLE

## BACKGROUND OF THE INVENTION

This invention relates generally to battery saving methods suitable for use with radio paging communications systems, and more particularly to radio paging communications systems which include selectively called paging receivers which have assignable battery saver duty cycles.

Radio paging communications systems which include selectively called paging receivers having battery saving operation are in widespread use today. Both tone coded and digital coded battery saving schemes are in use, providing a variety of system battery saving performance characteristics. These current communications systems have generally provided adequate battery saving operation for paging receivers which utilize N-cell size and larger batteries. However, the small physical size and form factor of paging devices, such as wrist worn pager/watch devices, preclude the use of batteries larger than button cells. Thus while battery saving performance is adequate in systems with the paging receivers incorporating substantial batteries, these systems are inadequate for paging devices operating from extremely limited energy sources, such as button cell batteries.

One solution to this problem, which has been proposed, is to simply extend the time period during which the pager/watch device is operating at reduced power consumption levels. Such a system limits device operation to only a brief time interval in

perhaps a much longer time interval of perhaps fifteen minutes. Such a system as described would not have broad appeal, as most knowledgable paging users expect system response times, i.e. the time period between when a paging call has been entered to the time when the paging call is received by the paging receiver, to be on the order of two minutes or less. Implementation of a solution such as has been proposed would increase the system response times throughout a paging system, and would be totally unacceptable. The proposed system would also be very inefficient and costly, as extremely large paging call and message qeues would have to be provided in the terminal handling the paging calls. Such a solution is not only expensive, but is sure to create tremendous customer dissatisfaction. Clearly, short message qeues and rapid system response times must be maintained throughout the system as a whole. The problem is how to satisfy these needs, and balance them with the requirement of adequate battery life cycles for all paging receivers in the system, including those paging devices operating from extremely limited energy sources.

## SUMMARY OF THE INVENTION

It is an object of the present invention to provide a system and apparatus providing improved battery life for paging receivers.

It is a further object of the invention to provide a system and apparatus which provides selective battery life improvement based on the battery in use.

It is a further object of the invention to provide a system and apparatus which maintains system throughput, while providing the selective battery life improvement.

It is a further object of the invention to provide a system and apparatus which minimizes the penalty of operating a paging receiver with a battery of limited energy content.

It is a further object of the invention to provide a system and apparatus which provides a multiplicity of battery saving performances which are selectable at both the terminal and the paging receiver.

It is a further object of the invention to provide a system and apparatus which provides assignable battery saving operation using the paging device's address.

It is a further object of the invention to provide a system and apparatus which allows multiple battery saver duty cycles to be intermixed in the same system.

These and other objects and advantages of the present invention will become apparent to those skilled in the art upon consideration of the following description and accompanying drawings of the invention.

## BRIEF DESCRIPTION OF THE DRAWINGS

The features of the invention which are believed to be novel are set forth with particularity in the appended claims. The invention itself, together with further objects and advantages thereof, may be best understood by reference to the following description when taken in conjunction with

the accompanying drawings, in the several figures of which like reference numerals identify identical elements, in which:

FIGS. 1A - 1C comprise descriptive diagrams for a conventional battery saving system.

FIGS. 2A - 2C comprise descriptive diagrams for a battery saving system employing a coded sync signal in accordance with the present invention.

FIGS. 3A - 3D comprise descriptive diagrams for a battery saving system illustrating the operation of a paging receiver employing a coded sync signal in accordance with the present invention.

FIG. 4 is a simplified electrical schematic diagram of the preferred embodiment of the present invention.

FIG. 5 is a functional diagram of a microcomputer utilized in the preferred embodiment of the present invention.

FIGS. 6A - 6C are flowcharts describing the operation of the preferred embodiment of the present invention.

## DESCRIPTION OF THE PREFERRED EMBODIMENT

Reference is now directed to the drawings, and in particular to Fig 1. which illustrates one prior art battery saving method, in particular that used in the POCSAG signalling system, which is well known to those skilled in the art. The POCSAG code format, as shown in FIG. 1A, utilizes a digital code format and consists of batches of pages transmitted at regular intervals. Each batch is shown to consist of a sync word followed by the pages to be transmitted.

As can be seen in FIG. 1B, following the sync word, pages are transmitted in eight separate frames of address codes, namely 1-8, each of which includes two address segments. All pagers in the system are assigned to operate in one of the eight frames.

FIG. 1C shows an example of how battery saving is accomplished in the POCSAG signalling system. As shown in FIG. 1C, a pager has been assigned to frame 6. The pager intermitantly provides power to the receiver section for a period of time long enough to detect the sync word, thereby continuously maintaining synchronization with the system. After the sync word has been detected, power is removed from the receiver until the frame to which the pager has been assigned occurs, in this case, frame 6. Power is again supplied to the receiver section for the duration of frame 6 during which time the pager is evaluating the received addresses to determine if a page has been sent to it. If a page was not received during the assigned frame, power is again removed from the receiver until the next sync word is to be transmitted. Thus, the POCSAG signalling system provides approximately a one to eight battery saving ratio, i.e. the time the receiver is on to the time the receiver is off.

The POCSAG signalling system described thus provides a battery saving format which delivers the same effective battery saver duty cycle to all pagers in the system. Such a system does not provide a method of varying the duty cycle which is required to improve battery life, unless the entire system is changed.

In the preferred embodiment of the present invention, an improved battery saver system is shown in FIG. 2 which provides for a substantial improvement in battery life. While the basic format shown in FIG. 2A and 2B is similar to the prior art systems, the sync signal, or word, is no longer a single fixed word. Any number of distinct batches are created by including a coded sync word including a sync word and a sync I.D. at the end of the sync word as shown in FIG. 2C. The format of the sync I.D. can be of any number of forms, such as a four bit binary word ranging from 0 to 15. It will be appreciated by those skilled in the art that the number of sync I.D.'s provided in the system is a matter of choice, based upon the largest battery saving ratio contemplated for use in the system. Sync I.D.'s are assigned to a common sync word identifying each batch, and batches are transmitted in proper sequence.

In the example shown in FIG. 2A there are N coded sync words describing N different batches to which pagers can be assigned. Unlike the prior art system, where pagers are assigned only to a single frame, in the preferred embodiment of the present invention, pagers can be assigned to a frame transmitted in one or more of the N different batches previously described, thereby tailoring the battery saver duty cycle to the type of pager in service.

The improvement potentially obtainable can best be appreciated by considering a number, such as sixteen coded sync words, defining sixteen unique transmittable batches. FIG. 3 illustrates the flexibility of the battery saving system described.

In the preferred embodiment of the present invention, pagers can be assigned to operate in one, or any combination of unique batches, or sync groups, defined by the coded sync words assigned. If a pager is assigned in a conventional manner to receive pages during frame six, and specifically only during sync group two, as shown in FIG. 3B, then the pager will only turn on one out of 128 possible frames, for a battery saver duty cycle of 1:128. If the pager is assigned to two of the possible sync groups as shown in FIG. 3C, the pager turns on for two of the possible 128 frames, for a battery saver duty cycle of 1:64. It is possible to assign a pager to all sync groups as shown in FIG. 3D with a resultant battery saver duty cycle of 1:8, which is the same as provided by the prior art POCSAG code format.

As will be appreciated by those skilled in the art, the sync groups to which a pager will respond can be individually assigned and stored in the pager in the same manner as individual addresses are assigned to the pagers. The terminal normally used to queue pages in the correct frame in which they are to be transmitted, would also queue the pages by the sync groups to which the individual pagers are programmed to respond. Pagers providing different battery saver duty cycles can be mixed on the same system without interfering with each other. Pagers, such as miniature wrist worn pagers, could be assigned to long battery saving duty cycles, while other pagers could be assigned to a shorter battery saving duty cycle, such as the prior art battery saving duty cycle.

Figure 4 shows an electrical block diagram of a pager constructed in accordance with the present invention. The pager 20 includes an antenna 22 and a receiver portion 24 used to receive the transmitted coded sync signals and pages, or addresses, to which the pager will respond, in a manner well known to those skilled in the art. The demodulated signals corresponding to the transmitted coded sync signals and addresses are presented as a bit stream of binary information 25 at the output of receiver 24.

As will be appreciated by those skilled in the art, the functions shown as a bit pattern detector 28, control logic 32, and programmable timer 36 may be readily implemented using a microcomputer 26. The binary information bit stream 25 is applied to bit pattern detector 28 of microcomputer 26 where the signals are compared with the sync groups and address codes, which are stored in address memory 30, to maintain system synchronization, to determine the time to the next assigned sync group, and to detect pages directed to the pager.

The sync group and address codes are assigned to the pager by programmiing them into address memory 30 in a manner well known to those skilled in the art. Address memory 30 may be reprogrammable, such as an EEPROM memory, thereby allowing sync groups or addresses to be readily implemented and changed.

Control logic 32 of microcomputer 26 interfaces to address memory 30 and to bit pattern detector 28 controlling the comparison of received sync codes with those stored in address memory 30. A crystal oscillator 34 provides the clock necessary for control logic 32 portion of microcomputer 26. An

output of crystal oscillator 34 also provides a reference clock for programmable timer 36 of microcomputer 26. Programmable timer 36 generates the interval signals which are supplied to bit pattern detector 28 and control logic 32, allowing control of when the bit detector correlates for either the sync group, or addresses in any transmitted batch. The time intervals generated by the programmable timer 36 are controlled by control logic 32 corresponding to the sync groups stored in address memory 30. Thus, once the pager has achieved synchronization with the system, the pager battery saver will not supply power to the receiver unless it is during one of the sync groups to which the pager is assigned to operate.

Power to the receiver 24 is controlled in a manner well known to those skilled in the art by the battery saver circuit 38 which is controlled by battery saver signal 31 which is generated by control logic 32 in a manner corresponding to the battery saver operation defined by the sync codes stored in address memory 30. An output annunciator 40 is provided, which may be an LCD display in the case of a display pager, or a transducer in the case of a tone only pager, for alerting the user when a page has been received.

To recap briefly, a pager has been described in FIG. 4 corresponding to the preferred embodiment of the present invention which provides assignable battery saver duty cycles. The pager is capable of operating in any combination of sync groups, and battery saver operation is defined by sync codes stored in the pager address memory, thereby insuring no operation of the battery saver circuit, except

during those sync group time intervals to which the pager is programmed.

Reference is now directed to FIG. 5 which shows a functional block diagram of microcomputer 26 which contains the firmware for implemention of assignable battery saver duty cycles. In the preferred embodiment of the invention as herein shown, the microcomputer is a Motorola 146805 type. U.S. Patent Number 4,518,961 entitled "Universal Paging Device with Power Conservation", owned by the same assignee of this invention, discloses the use of such a microcomputer. The disclosure of this patent is hereby incorporated by reference.

The bit clock signal from crystal oscillator 34 is suppled to a timer control unit 80 containing a prescaler and a timer and counter. An output of crystal oscillator 32 is also connected to a central processing unit (CPU) 82 which contains the central processing unit control circuit, an arithmetic logic unit designated ALU, an accumulator, index register, condition code register, stack pointer, program counter high and program counter low modules. Also connected to the central processing unit are data directional input/output (I/O) registers 86 and 86 having a plurality of input/output lines. In particular, eight lines are shown for each of two input/output ports.

As indicated, an output line of register 84 is connected to line 31 to provide control of battery saver circuit 38. An input line of register 84 is connected to receive the binary information bit stream signal 25 from receiver 24. An output line of register 86 is connected to output annunciator 40.

Four I/O lines of register 86 are connected to address code memory 30.

Also interfacing with the central processing unit are a read-only memory (ROM) 88 and a random access memory (RAM) 90. As is characteristic of the Motorola 146805 family, the on-chip RAM permits microcomputer 26 to operate without an external RAM memory. The parallel input/output capability includes programmable pins indicating whether it is to be an input or an output. The timer/counter 80 is normally an eight bit counter with a programmable prescaler which can be used as an event counter to generate interrupt signals at certain software-selected events or can by used for keeping timing.

FIG. 5 also shows the arrangement of major firmware modules stored in ROM 88. The choice and arrangement of this module is a function of the specific program of the embodiments of the present invention. The use of RAM 90 is pricipally to contain variables accessed during the program and as a scratch-pad storage.

The 146805 microcomputer and its asscociated architecture and internal instruction set have been described in detail in the following U.S. patents and applications: U.S. Serial Number 054,093, filed July 2, 1979, entitled "Low Current Input Buffers"; U.S. Serial Number 065,292, filed August 9, 1979, entitled "Method for Reducing Power Consumed by a Static Microprocessor"; U.S. Serial Number 065,293, filed August 9, 1979, entitled "Apparatus for Reducing Power Consumed by a Static Microprocessor"; U.S. Patent Number 4,300,195, filed August 9, 1979, entitled "CMOS Microprocessor Architecture"; U.S.

Patent Number 4,280,190, filed August 9, 1979, entitled "Incrementor/Decrementor Circuit"; and U.S. Patent Number 4,308,581, filed September 28, 1979, entitled "A Single Step System for a Microcomputer", all of the above six patents and applications being commonly assigned to the assignee of the present invention. The six designated patents and applications are hereby incorporated by reference for a more complete description of the MC146805 microcomputer.

Reference is now directed to FIGs. 6A-C which are flowcharts describing the operation of the battery saving circuit for the preferred embodiment of the present invention. As illustrated in flow chart 300 of FIG. 6A, the system is first initialized, as shown at block 302. Next the code plug, or address, memory is read, as shown at block 304, the result of which is utilized to initialize the timing, such as shown at block 306. A search for bit sync is initiated, as shown at block 308. If bit sync is not found, the search routine is re-initiated. If bit sync is found, bit timing is established, as shown at block 310, which in turn is effective to start a time-out timer for detecting a sync word, as shown at block 312, which is used to effect the search for a sync word, as shown at block 314. If a sync word is not detected, as shown at block 314, the search will continue for a predetermined time, as shown at block 316, after which the routine reverts back to search for bit sync, as shown at block 308.

When a sync word is detected, as shown at block 314 of FIG. 6A, the sync I.D., or sync group, is extracted and loaded into the sync group timer, as

shown at block 354 of FIG. 6B. The sync group timer value is correlated with the sync groups assigned to the unit. If the sync group is not one of the sync groups assigned to the unit as shown at block 355, the timer is set up for the time to the next assigned sync group as shown at block 356. When sync group time-out occurs as shown at block 358, a search for the next assigned sync word is initiated, as shown at block 360. If the assigned sync word is not detected, indicating the sync word has been missed, as shown at block 360, the sync word flag is read, as shown at block 362. If the sync word detect flag was set, as shown at block 364, it indicates a second miss of sync word detection has occured, as shown at block 370, and a search for bit sync is re-initiated, as shown at block 308 of FIG. 6A.

If the sync word detect flag was not set, as shown at block 364, then this was the first time sync word was missed, and the sync word detect flag is set, as shown at block 366. Address decoding then begins at point B, as shown in FIG 6C. Similarly, if the sync word was detected during the sync word search, as shown at block 360, address decoding begins at point B, as,shown in FIG 6C.

When address decoding begins, the timer is set up for address decoding, as shown at block 338, in FIG. 6C. When the timer times-out, as shown at block 340, indicating the proper frame is present in which to search address, the address search is begun, as shown at block 342. If the address is not detected, as shown at block 342, the group sync timer is set up for the next assigned group sync interval, as shown at block 356 of FIG. 6B.

When an address is detected, as shown at block 342 of FIG. 6C, the function bits are decoded, as shown at block 344. If the function bit indicates no message was transmitted, indicating a tone only page, as shown at block 346, an alert signal is generated, as shown at block 348. The group sync timer is set up for the next group sync interval, as shown at block 356 of FIG. 6B.

When the function bits indicate a message was received, as shown at block 346, the received message is stored, as shown at block 350, and an alert is generated, as shown at block 352. The group sync timer is set up for the next group sync interval, as shown at block 356 of FIG. 6B.

To recap briefly, a procedure for providing a flexible battery saving system utilizing assignable battery saver duty cycles has been described. It will be appreciated by those skilled in the art, that the procedure and apparatus described allows mixing of pagers with different battery saver duty cycles on a single system without interference. It will also be appreciated by those skilled in the art, that the procedure and apparatus described allows battery saving to be optimized to the type of battery provided in the pager.

CLAIMS:

1. A selective call communications system, comprising:

transmitter means for transmitting selective call signals in a predetermined signalling format;

a first group of selective call receivers for receiving and decoding the selective call signals transmitted in the predetermined signalling format from said transmitter means, each of said receivers having a battery saver circuit for periodically providing power to the receiver at a first repetition rate;

a second group of selective call receivers for receiving and decoding the selective call signals transmitted in the predetermined signalling format from said transmitter means, each of said receivers having a battery saver circuit for periodically providing power to the receiver at a second repetition rate.

2. The selective call communications system according to claim 1, wherein:

said transmitter means transmits selective call signals to said first group of receivers when said first group of receivers is powered; and

said transmitter means transmits selective call signals to said second group of receivers when said second group of receivers is powered.

3. A receiver comprising:

means for receiving and demodulating transmitted coded signals, the coded signals including a plurality of coded sync signals sequentially transmitted at predetermined time intervals;

means for storing assigned sync identification information corresponding to the assigned sync words;

means to derive sync signals and sync identification information from the demodulated coded signals;

means for computing the time interval from the currently derived coded sync signal to the next assigned coded sync signal; and

battery saving means responsive to said means for computing the time for suspending the supply of power to the receiver until the next assigned coded sync signal.

4. A method for providing an assignable battery saver duty cycle to a communications receiver operating in a communications system, wherein transmitted coded signals are received by the receiver, the transmitted coded signals including a plurality of coded sync signals sequentially transmitted at a predetermined time interval, each coded sync signal including a sync word and sync identification information, and wherein the communications receiver includes a memory storing assigned sync identification information corresponding to the next assigned sync word, and further has means for controlling the supply of power from a battery to the receiver, said method comprising:

continuously supplying power to the receiver;

detecting and deriving sync and sync identification information;

computing the time interval to the next transmitted coded sync word corresponding to the next assigned sync word; and

suspending the supply of power to the receiver for the duration of the time interval to the next assigned coded sync word, whereby synchronization to the system is established and battery save operation is initiated.

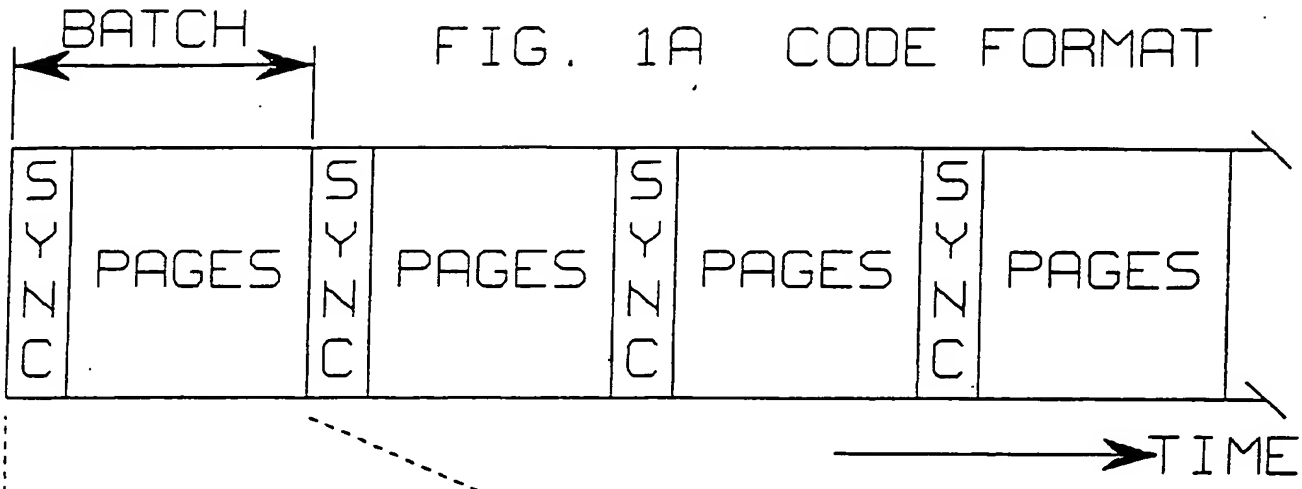



FIG. 1A CODE FORMAT

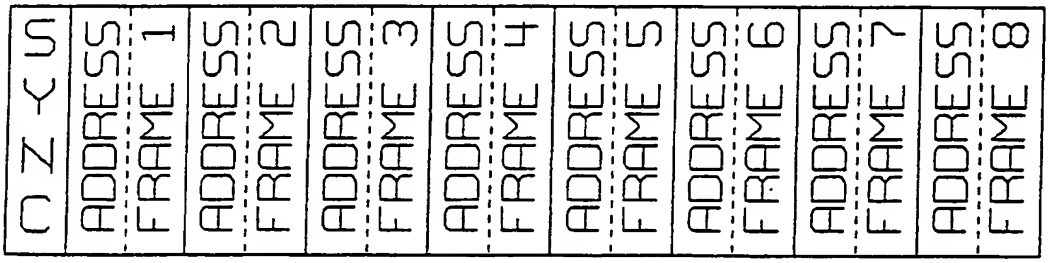



FIG. 1B FRAME FORMAT

FIG. 1C
BATTERY SAVER TIMING FOR
PAGER IN GROUP 6

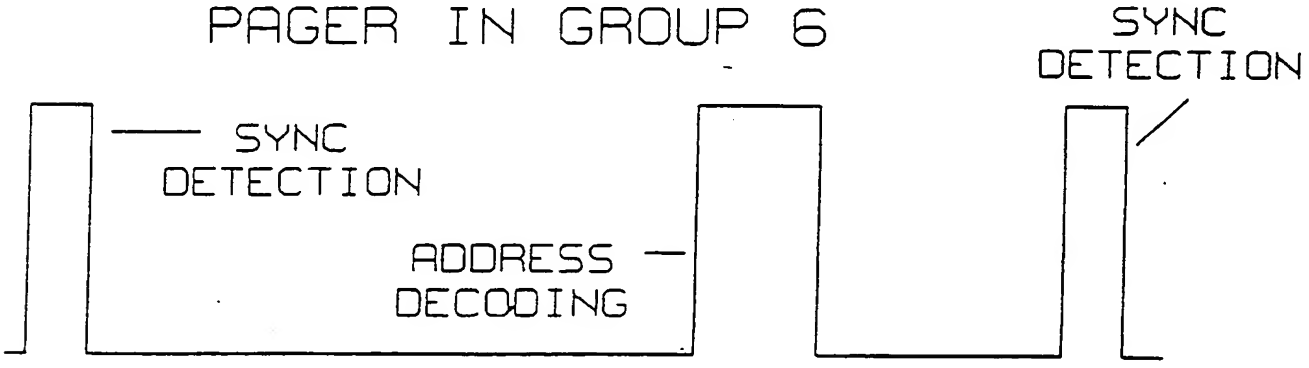



FIGURE 1
POCSAG SIGNALLING SYSTEM

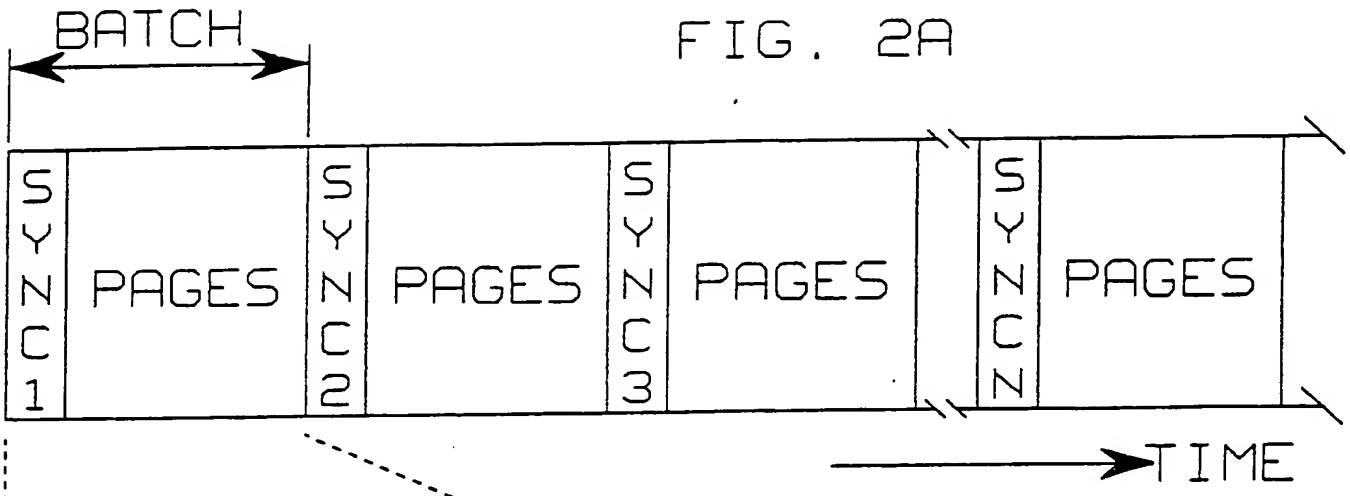



FIG. 2A

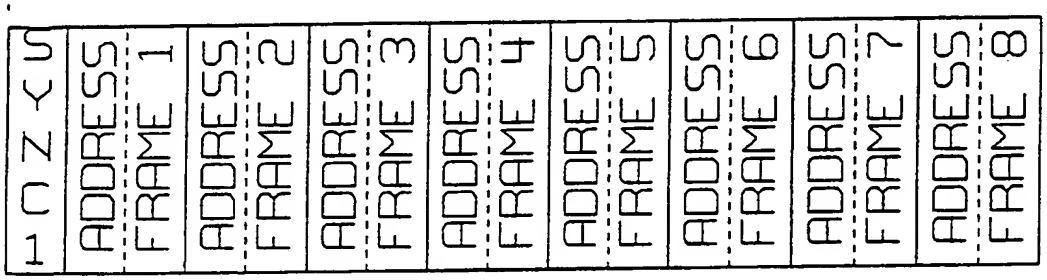



FIG. 2B

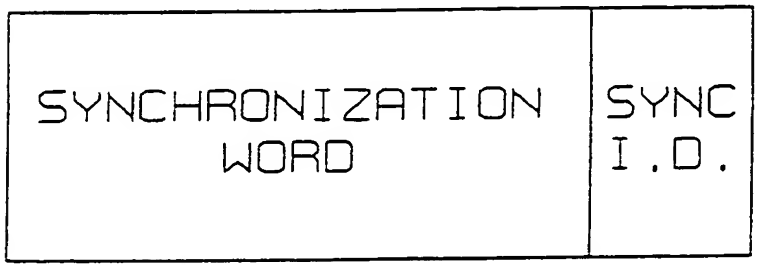
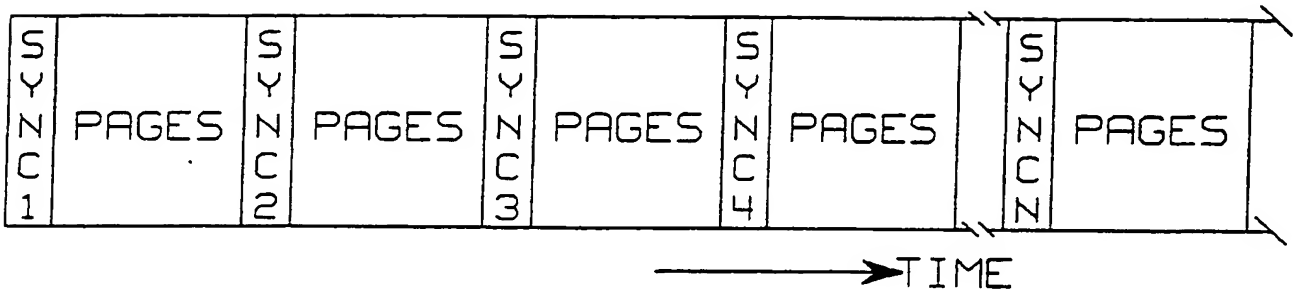



FIG. 2C

FIG. 3A



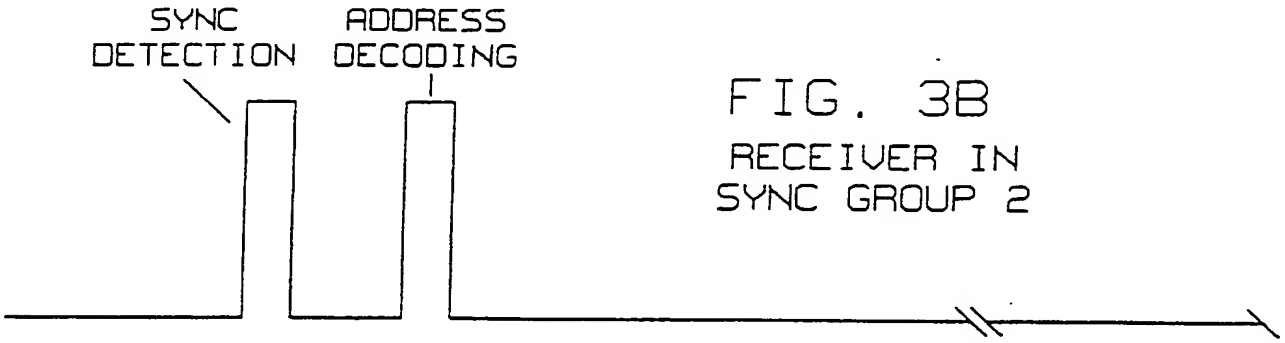




FIG. 3B
RECEIVER IN SYNC GROUP 2

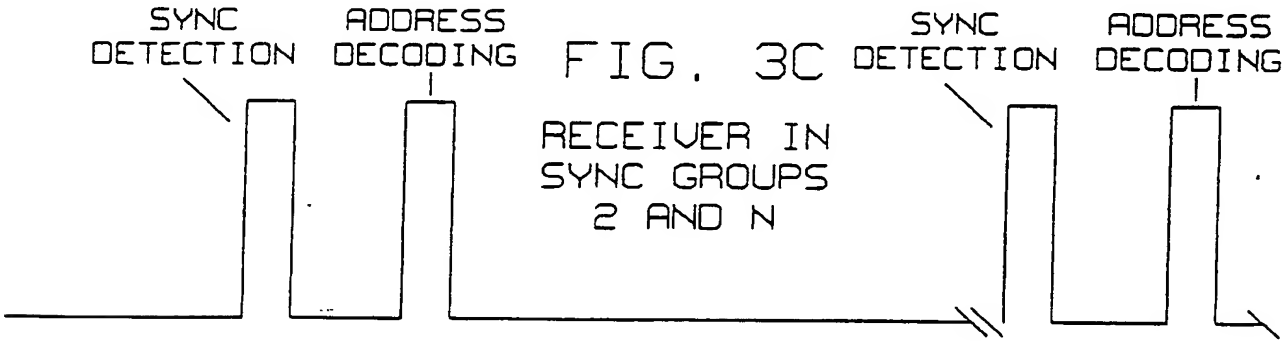



FIG. 3C
RECEIVER IN SYNC GROUPS 2 AND N

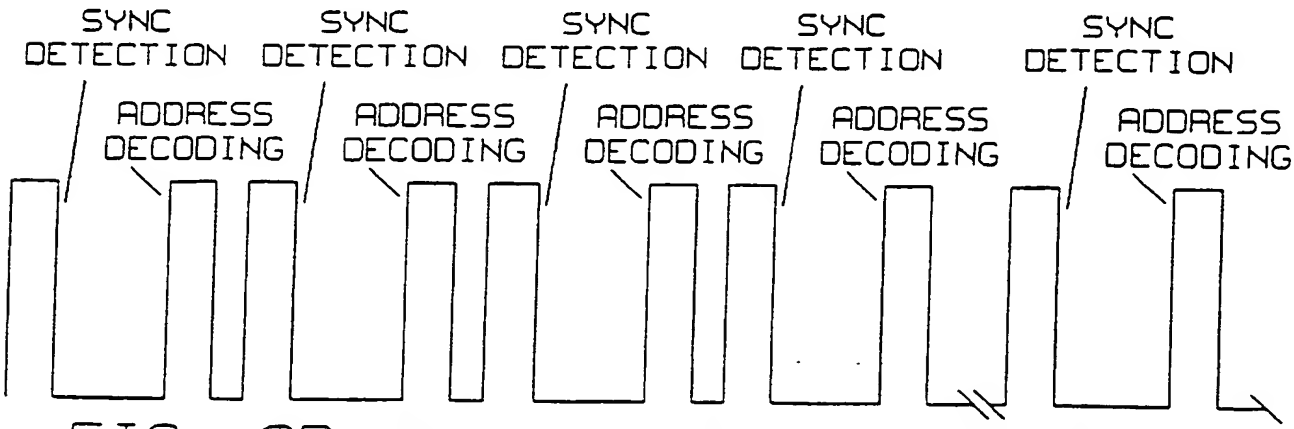



FIG. 3D RECEIVER IN ALL SYNC GROUPS

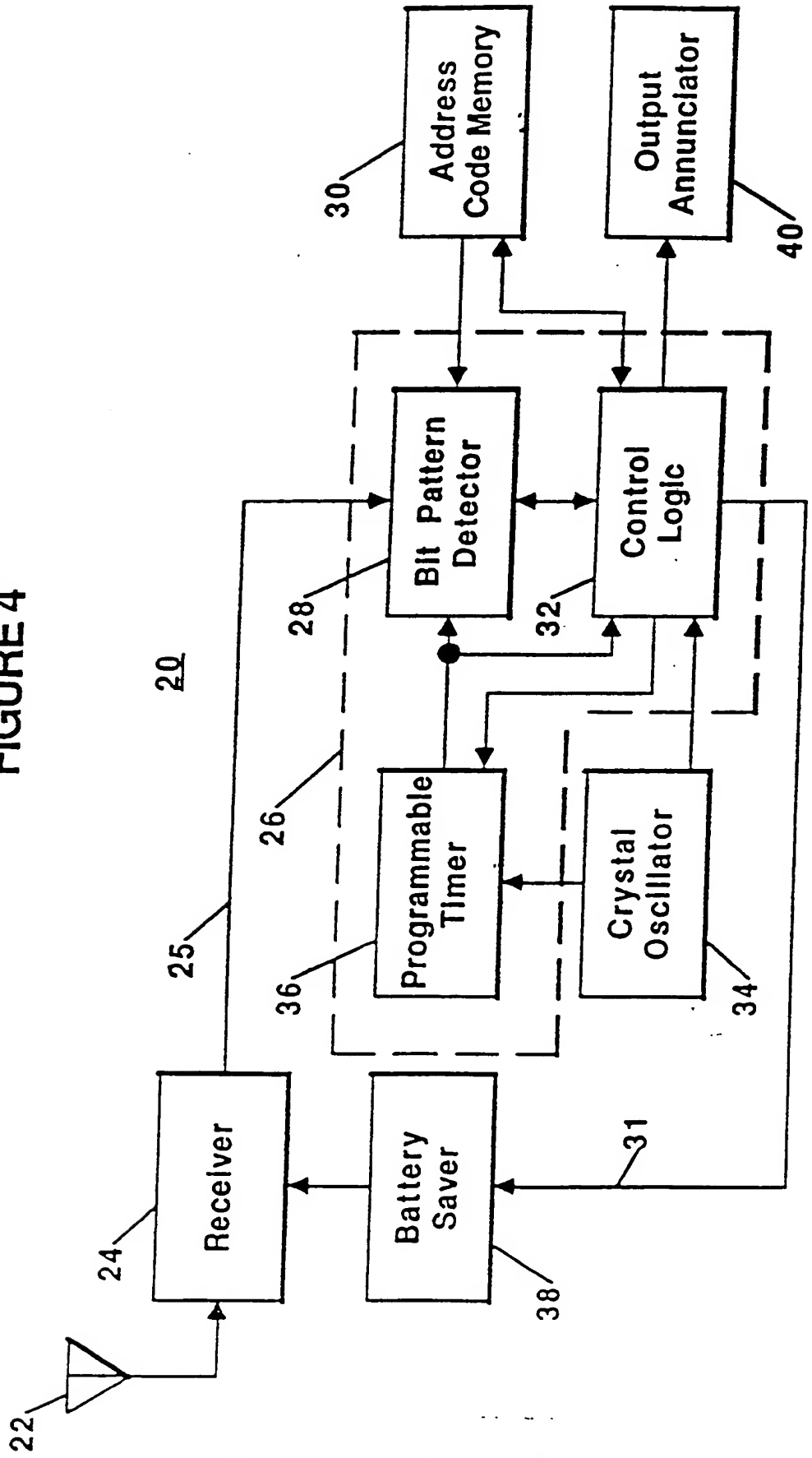

Address Code Memory
30
Output Annunciator
40
Bit Pattern Detector
28
Control Logic
32
20
26
Programmable Timer
36
Crystal Oscillator
34
25
Receiver
24
Battery Saver
38
31
22

FIGURE 4

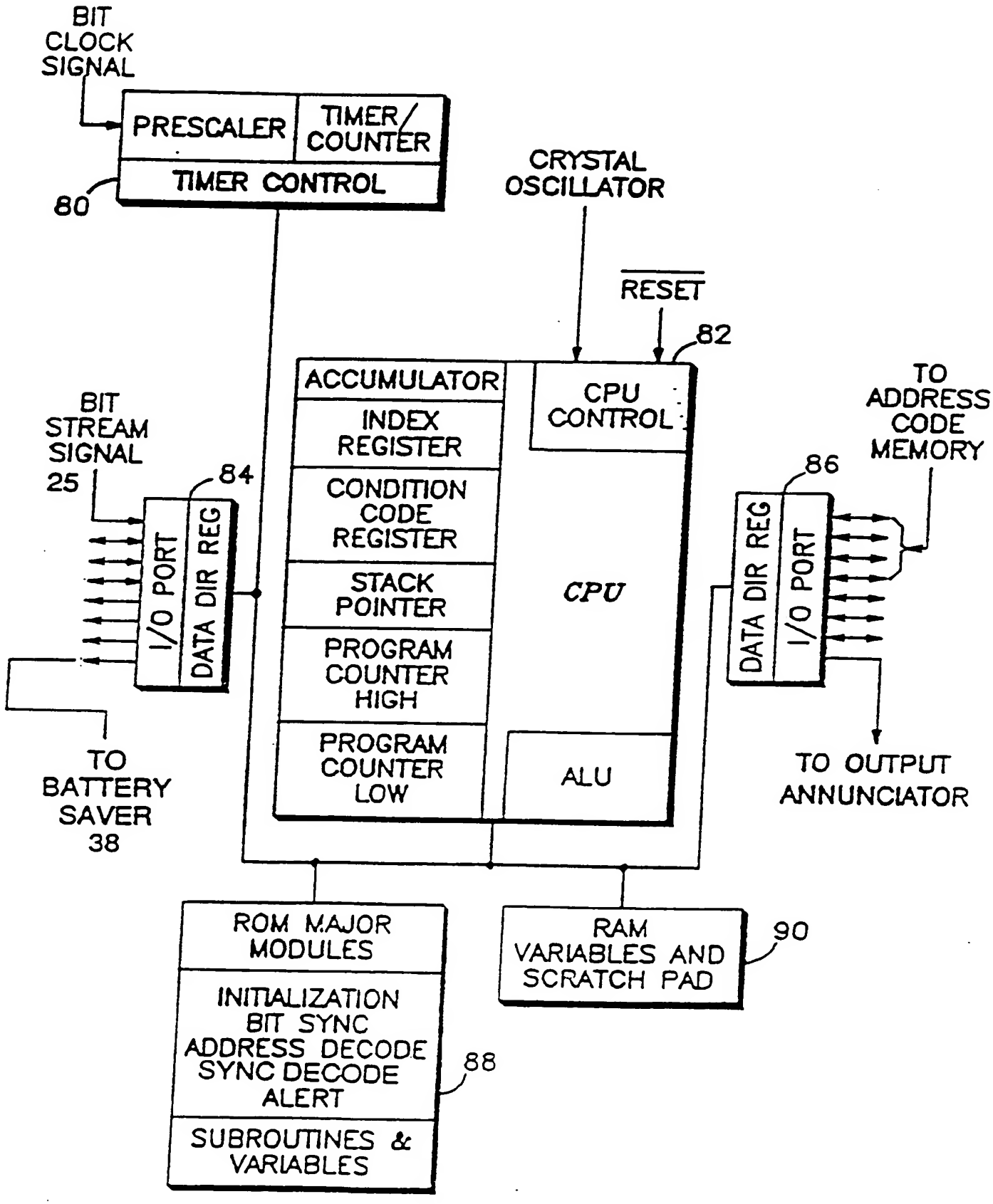

BIT CLOCK SIGNAL
PRESCALER
TIMER/ COUNTER
TIMER CONTROL
80
CRYSTAL OSCILLATOR
RESET
82
ACCUMULATOR
INDEX REGISTER
CONDITION CODE REGISTER
STACK POINTER
PROGRAM COUNTER HIGH
PROGRAM COUNTER LOW
CPU CONTROL
CPU
ALU
BIT STREAM SIGNAL
25
84
I/O PORT
DATA DIR REG
TO BATTERY SAVER 38
TO ADDRESS CODE MEMORY
86
DATA DIR REG
I/O PORT
TO OUTPUT ANNUNCIATOR
ROM MAJOR MODULES
INITIALIZATION
BIT SYNC
ADDRESS DECODE
SYNC DECODE
ALERT
88
SUBROUTINES & VARIABLES
RAM VARIABLES AND SCRATCH PAD
90

FIG. 5

FIG. 6A

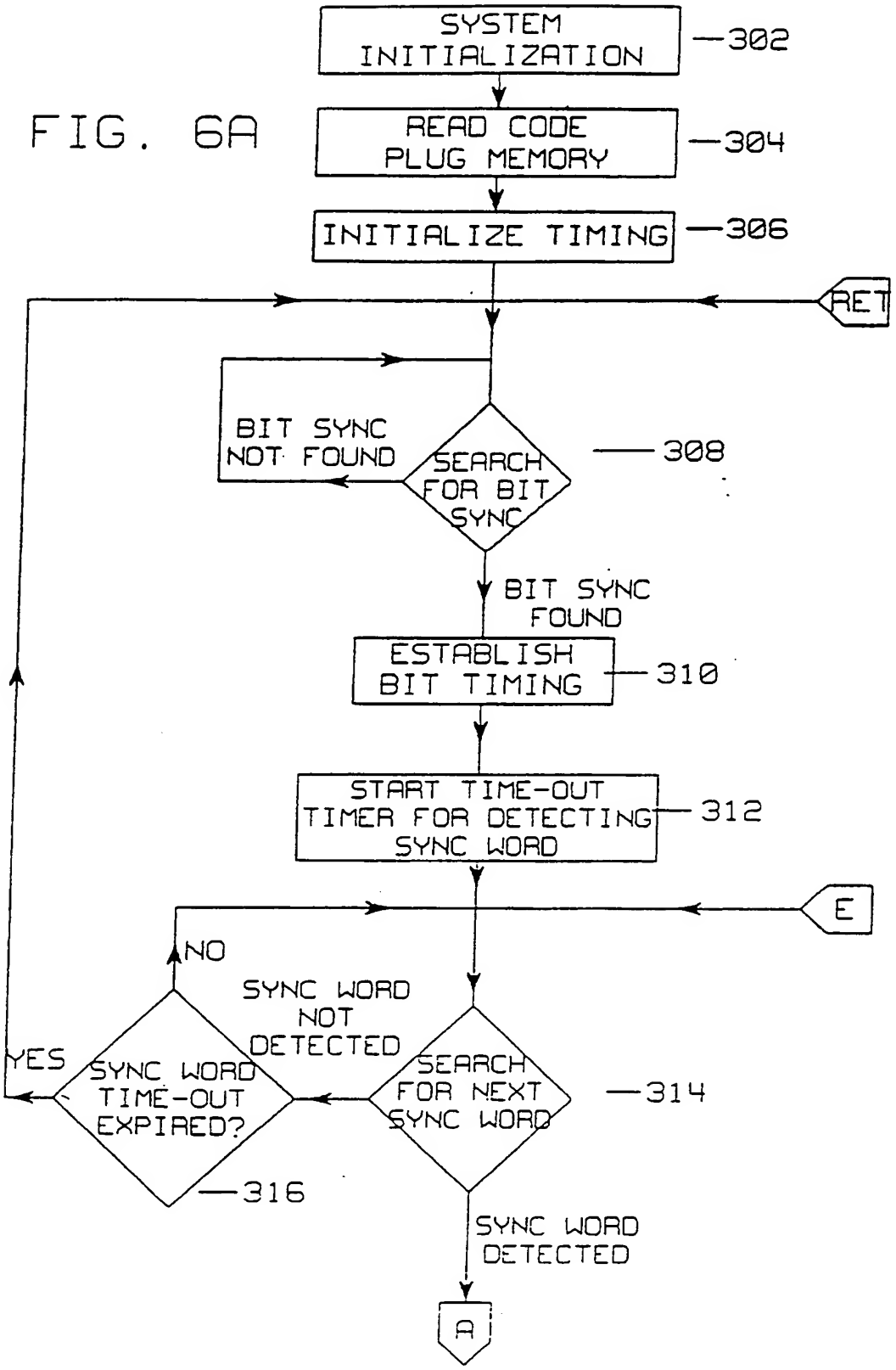

SYSTEM INITIALIZATION
302
READ CODE PLUG MEMORY
304
INITIALIZE TIMING
306
RET
BIT SYNC NOT FOUND
SEARCH FOR BIT SYNC
308
BIT SYNC FOUND
ESTABLISH BIT TIMING
310
START TIME-OUT TIMER FOR DETECTING SYNC WORD
312
E
NO
SYNC WORD NOT DETECTED
YES
SYNC WORD TIME-OUT EXPIRED?
316
SEARCH FOR NEXT SYNC WORD
314
SYNC WORD DETECTED
A

FIG. 6B

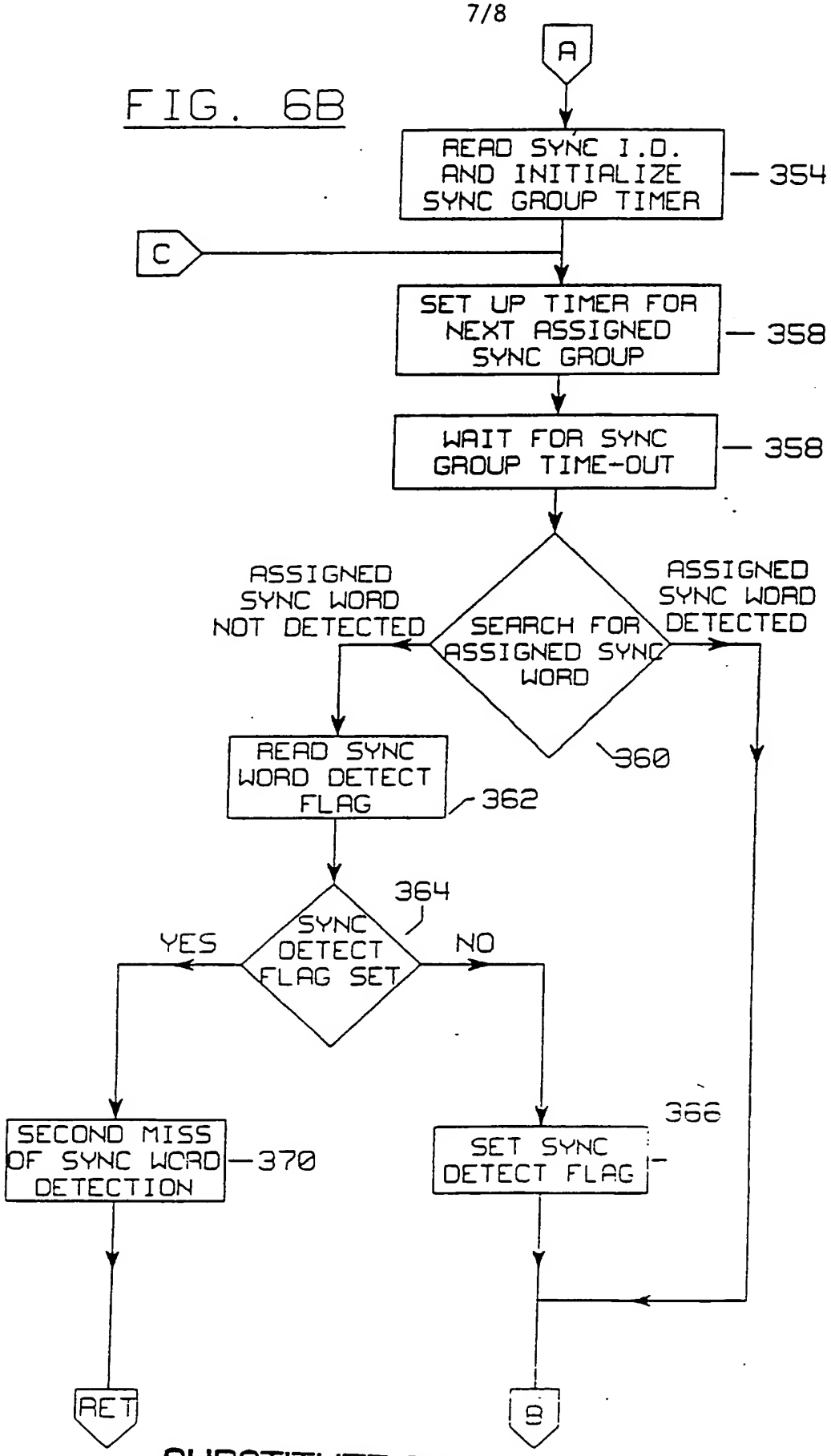
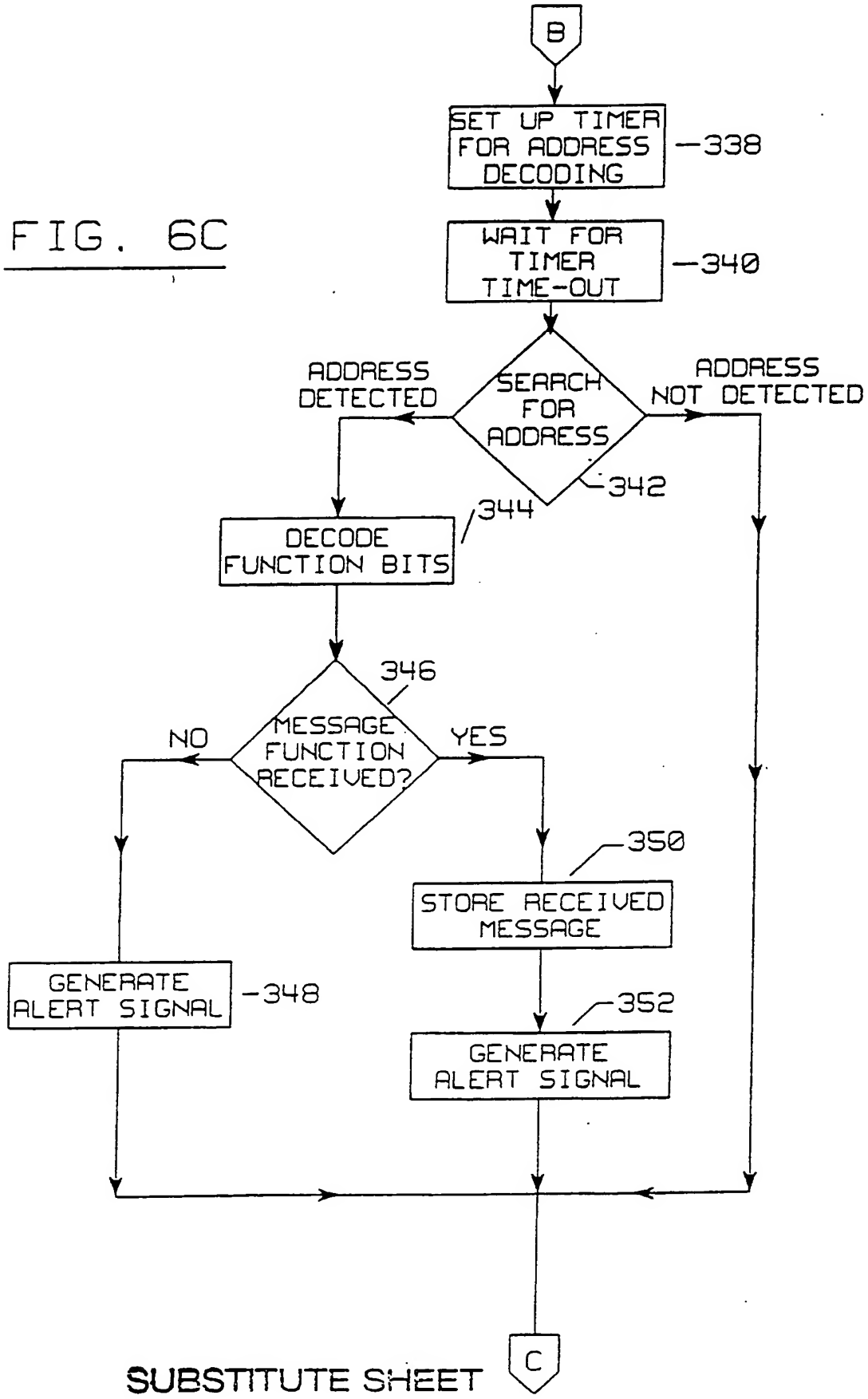

A
READ SYNC I.D. AND INITIALIZE SYNC GROUP TIMER
354
C
SET UP TIMER FOR NEXT ASSIGNED SYNC GROUP
358
WAIT FOR SYNC GROUP TIME-OUT
358
ASSIGNED SYNC WORD NOT DETECTED
SEARCH FOR ASSIGNED SYNC WORD
ASSIGNED SYNC WORD DETECTED
360
READ SYNC WORD DETECT FLAG
362
364
SYNC DETECT FLAG SET
YES
NO
SECOND MISS OF SYNC WORD DETECTION
370
366
SET SYNC DETECT FLAG
RET
B

FIG. 6C


B
SET UP TIMER FOR ADDRESS DECODING
338
WAIT FOR TIMER TIME-OUT
340
SEARCH FOR ADDRESS
342
ADDRESS DETECTED
ADDRESS NOT DETECTED
DECODE FUNCTION BITS
344
346
MESSAGE FUNCTION RECEIVED?
NO
YES
GENERATE ALERT SIGNAL
348
350
STORE RECEIVED MESSAGE
352
GENERATE ALERT SIGNAL
C

# INTERNATIONAL SEARCH REPORT

International Application No PCT/US 87/00005

## I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) *

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[4]: H 04 Q 7/02; H 04 B 1/16

## II. FIELDS SEARCHED

Minimum Documentation Searched 7

| Classification System | Classification Symbols |
|---|---|
| IPC[4] | H 04 B, H 04 Q |

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched *

## III. DOCUMENTS CONSIDERED TO BE RELEVANT *

| Category * | Citation of Document, 11 with indication, where appropriate, of the relevant passages 12 | Relevant to Claim No. 13 |
|---|---|---|
| X | GB, A, 2115195 (GENERAL ELECTRIC COMPANY) 1 September 1983 see page 3, line 47 - page 5, line 57; figures 1-4 | 1,2 |
| X | EP, A, 0124788 (NEC CORPORATION) 14 November 1984 see page 4, line 20 - page 19, line 22; figures 1-5 | 1,2 |
| A | | 3,4 |
| X | Patent Abstracts of Japan, vol. 6, no. 111(E-114)(989), 22 June 1982 see the abstract, & JP, A, 5741045 (MATSUSHITA DENKI SANGYO K.K.) 6 March 1982 | 1,2 |
| Y | | 3,4 |
| Y | Patent Abstracts of Japan, vol. 2, no. 99(E-78)(4877), 17 August 1978 see the abstract, & JP, A, 5363905 (NIPPON DENSHIN DENWA KOSHA) 6 July 1978 | 3,4 |

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* Special categories of cited documents: 10

"A" document defining the general state of the art which is not considered to be of particular relevance

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

## IV. CERTIFICATION

| Date of the Actual Completion of the International Search | Date of Mailing of this International Search Report |
|---|---|
| 10th September 1987 | 21 OCT 1987 |
| International Searching Authority | Signature of Authorized Officer |
| EUROPEAN PATENT OFFICE | M. VAN MOL |

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

| Category.* | Citation of Document, with indication, where appropriate, of the relevant passages | Relevant to Claim No |
|---|---|---|
| A | Patents Abstracts of Japan, vol. 6, no. 111 (E-114)(989), 22 June 1982 see the abstract; & JP, A, 5741044 (MATSUSHITA DENKI SANGYO K.K.) 6 March 1982 -- | 3,4 |
| A | Patents Abstracts of Japan, vol. 4, no. 162 (E-33) (644), 12 November 1980 see the abstract; & JP, A, 55110441 (NIPPON DENKI K.K.) 25 August 1980 -- | 3,4 |
| A | Japan Telecommunications Review, vol. 19, no. 3, July 1977 (Tokyo, JP) M. Komura et al.: "New Radio Paging System", pages 217-225, see pages 221-222, paragraph 5.1; figure 6 -- | 3,4 |
| A | International Zurich Seminar on digital Communications, 4-6 March 1980 (Zürich, CH) R.H. Tridgell: "The application of coding techniques to radiopaging", pages C9.1-C9.5, see page C9.2, paragraph 4.3, page C9.3, paragraph 5.2 | 3,4 |

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ANNEX TO THE INTERNATIONAL SEARCH REPORT ON

INTERNATIONAL APPLICATION NO. PCT/US 87/00005 (SA 15838)

This Annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 07/10/87

The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

| Patent document cited in search report | Publication date | Patent family member(s) | | Publicati date |
|---|---|---|---|---|
| GB-A- 2115195 | 01/09/83 | SE-A- | 8300425 | 02/08/83 |
| | | DE-A- | 3302849 | 11/08/83 |
| | | JP-A- | 58141035 | 22/08/83 |
| | | US-A- | 4449248 | 15/05/84 |
| EP-A- 0124788 | 14/11/84 | JP-A- | 59188247 | 25/10/84 |
| | | JP-A- | 59188248 | 25/10/84 |